University of Computer Studies, Yangon
B.C.Sc./B.C.Tech.

CT-404	**: Computer Architecture II**	**Second Semester**
Text Book	**:** Computer Architecture and Organization (3rd Edition) by John P. Hayes	
Period	**: 45** periods for 15 weeks (3 periods/week) (Lecture + Lab)	

Course Objectives

- To conceptualize the basics of organizational and architectural issues of a digital computer.
- To study the different ways of communicating with I/O devices and standard I/O interfaces.
- To study the hierarchical memory system including cache memories and virtual memory.
- To study various classes of instruction: data movement, arithmetic, logical, and flow control.
- To appreciate how conditional operations are implemented at the machine level.
- To understand the way in which subroutines are called and returns made.
- To understand parallelism both in terms of a single processor and multiple processors.

Learning Outcomes

The major outcomes of this course can be listed as

- Ability to perform computer arithmetic operations and control unit operations.
- Interpret the difference between hardwired and micro-programmed design approaches in CPU control unit design.
- Ability to understand the concept of I/O organization.
- Ability to conceptualize instruction level parallelism.
- Demonstrate the organization of memory hierarchy.
- Understand parallelism both in terms of a single processor and multiple processors.
- Understand how computer hardware has evolved to meet the needs of multi-processing systems.

Assessment Plan for the Course

Paper Exam: 60%

Attendance: 10%

Test/ Quiz: 10%

Lab: 10%

Lab Assessment: 10%

Tentative Lecture Plan

No.	Chapter		Page	Period	Examples and Problems
	Chapter 5	**Control Design**	332-399	**16**	
1.	5.2 5.2.1	Microprogrammed Control Basic Concepts	332-343	3	Eg. 5.4
2.	5.2.2	Multiplier Control Unit	344-353	3	Eg. 5.5
3.	5.2.3	CPU Control Unit	354-364	3	Eg. 5.6
4.	5.3 5.3.1	Pipeline Control Instruction Pipelines	364-371	2	Eg. 5.7
5.	5.3.2	Pipeline Performance	371-383	3	Eg. 5.8 Prob. 5.22 to 26
6.	5.3.3	Superscalar Processing	384-390	2	
	Chapter 6	**Memory Organization**	400-478	**20**	
7.	6.1 6.1.1 6.1.2	Memory Technology Memory Device Characteristics Random Access Memories	400-418	5	Eg. 6.1, 6.2 Prob. 6.1,4,5 Prob. 6.6, 7, 8, 9, 12
8.	6.1.3	Serial Access Memories	418-425	3	Eg. 6.3 Prob. 6.14, 15
9.	6.2 6.2.1 6.2.2	Memory Systems Multilevel Memories Address Translation	426-442	4	Eg. 6.4, 6.5 Prob. 6. 23 to 26
10.	6.2.3	Memory Allocation	443-452	3	Eg. 6.6, 6.7
11.	6.3 6.3.1	Caches Main Features	452-456	2	Prob. 6.30
12.	6.3.2 6.3.3	Address Mapping Structure versus Performance	457-471	3	Eg. 6.8 to 6.10
	Chapter 7	**System Organization**		**7**	
13.	7.1 7.1.1	Communication Methods Basic Concepts	480-491	1	Eg. 7.1

		Bus, Interconnection structure			
14.	7.1.2	Bus Control Basic features, Bus interfacing, Timing, Bus arbitration	491-501	2	Prob. 7.1, 5, 6
15.	7.2 7.2.1	I/O and System Control Programmed IO IO addressing	504-506	2	
16.	7.2.2	DMA and Interrupts	511-523	1	E.g. 7.4 Prob. 7.13
17.	7.2.3 7.2.4	I/O Processors IO instruction types Operating Systems	523-525 529-538	1	Overview
18.		Revision		**2**	